info@biopac.com
support@biopac.com
www.biopac.com

STP100D/STP100D-C ISOLATED DIGITAL INTERFACE

The STP100D module provides 16 bidirectional lines for digital input or output. All lines through the STP100D safely isolate connections to an MP160 or MP150 system up to 1500 volts.

The STP100D is used to safely isolate digital input and output lines to and from the MP System (MP160 and MP150).

The STP100D connects the MP System to computers running SuperLab, E-Prime, Inquisit, DirectRT, and other psychophysiological stimulation applications. The STP100D also includes output to drive solid state relay (0-3) and incorporates a BNC accessible External Trigger input line (TRIG).

The STP100D module can also be used to connect digital signals (standard logic level) from any mains powered external equipment to the MP System when the system also connects to electrodes attached to humans. STP100D Digital I/O card 37-pin connector pins (10-3) map to I/O15 - I/O8 on MP unit.

NOTE: *To interface the STP100D with devices that use BNC outputs, such as the fNIR System trigger ports, use the CBL125 BNC-to-BNC cable.*

Order based on the desired connection port type (depending on specific stimulus presentation software being used) to receive the correct interface cable:

STP100D includes CBL110A for SuperLab (uses Digital I/O card with 37 pin DSUB connector)

The STP100D optical interface can be used to interface to the MP System when SuperLab™ and the Digital I/O card with the Support Pack are already available. The STP100D interface connects between the SuperLab™ Digital I/O card and the AMI100D/HLT100C module to MP160. For MP150 see STP100C.

PORT A - To SuperLab: (pins 37-30) connect to MP System Digital I/O lines 0-7

PORT B - From SuperLab: (pins 3-10) connect to MP System Digital I/O lines 8-15

5 V power provided on pin 20

CBL110A

STP100D-C includes CBL110C for Parallel Port programs, e.g., E-Prime, DirectRT, MediaLab, Inquisit, or Vizard VR Toolkit (uses standard PC parallel port with DSUB 25 connector)

Pin assignments mimic a standard parallel port. The data register (typically used to send information from the host computer and thus generally used as inputs on the STP) is pins 2-9 with ground on pins 18 or 25. These pins correspond to digital channels 8-15 of the MP system. The STP can also communicate through the lines assigned to the status register, i.e., pins 10-13. These pins correspond to digital channels 4, 5, 7, and 6 respectively in the MP system.

CBL110C

Output Drives

The STP100D can drive up to four (4) solid state relays directly via the MP System Digital I/O lines 0-3 for relays or general-purpose logic level outputs.

The output drives (for relays or general-purpose logic level outputs) have 0 to 5 V output voltages and are current limited with 200 Ω resistors. This means that for solid state relay drive requirements, output current will be limited to approximately 20 mA, assuming an optically isolated solid state relay input diode drop of 1.2 V. Nearly all solid-state relays can operate with as little as 5 mA of current drive.

Digital Inputs

The STP100D is designed to work with digital inputs in the range of 0-3.0 V, 0-3.3 V and 0-5.0 V. The STP100D Digital inputs pull high and require current sinking ability of 4 ma to drive low. Digital high inputs must be greater than 2.5 V and Digital low input voltage must be less than 0.5 V.

MP160 Hardware with AMI100D

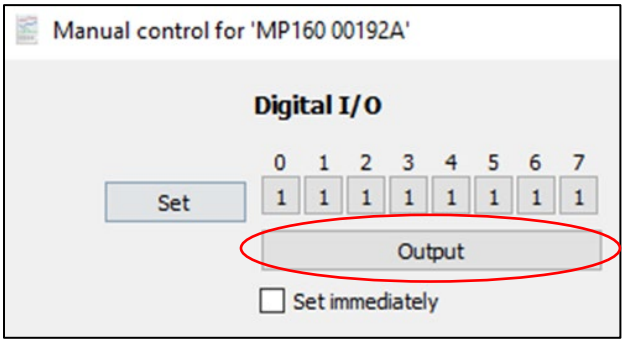
To enable an MP160 to recognize AMI100D and Smart Amplifier hardware, the digital channel for Smart Amplifier communication must be set high or undriven. The table below indicates which digital channel the system will use to communicate with Smart Amplifiers depending on the Rev number of the AMI100D. If connecting to hardware that affects this digital channel, third-party software (e.g., E-Prime, SuperLab) must be configured to allow the digital channel to remain high during three critical periods: (1) when Acq*Knowledge* is launched, (2) during channel setup when Acq*Knowledge* is asked to detect Smart Amplifiers, and (3) when the "Start" button is pressed either to commence acquisition or to begin waiting for a trigger.

The digital channel for Smart Amplifier communication depends on the Rev number of the AMI100D unit and the firmware version of the MP160. The Rev number can be found on the P-Touch label on the side of the device (see table below). BIOPAC also recommends that users update their Acq*Knowledge* to the latest version, which will also allow users to update the MP160 unit's firmware.

AMI100D Rev / MP160 firmware	Digital channel for Smart Amplifier communication
Any / earlier than 2.1.00	N/A (no communication
Any / earlier than 2.1.04	15
2 / 2.1.04 or later	
3 / 2.1.04 or later	7 with fallback to 15

NOTE:

Opening the manual control window and temporarily setting the lower digital channels to be outputs will allow the system to ignore the inputs.



If Smart Amplifiers are not detected by the system even with digital channels 7 and 15 held high by any external equipment attempting to drive them, it may be necessary to use a shorter cable between the STP100D and the external equipment. Users who have purchased USB-TTL may connect the device directly to the back of STP100D by removing the standoff screws from the gender changer included with the USB-TTL. BIOPAC is currently exploring other solutions to this issue.

info@biopac.com
support@biopac.com
www.biopac.com

Isolated External Trigger Input

The optically isolated external trigger input is standard logic level compatible. This line is accessible via a BNC female connector (labeled TRIG on the front of the STP100D)* and connects to the MP unit External Trigger input via optical isolation, compliant to 1500 VDC. The voltage range for this drive can support digital triggers in the range of 0-3.0 V, 0-3.3 V and 0-5.0 V.

*Alternatively, the isolated trigger input is also accessible via pin 12 of the DB-37 connector on the rear panel.

When the STP100D trigger is unused, it is pulled to a high state (+5 V) via an internal 100 kΩ resistor. To properly drive this line, connect a standard logic level driver to this port. For non-logic level type drivers, the low voltage applied to a trigger should ideally be between 0 and 1.0 V. The high voltage applied to the trigger should ideally be between 3.5 and 5 V. The maximum recommended source impedance of the driver should not exceed 1 kΩ. The trigger will accommodate logic levels anywhere in ±10 V range, but low level should be less than 1.0 V and high level should be greater than 3.5 V.

The pulse width to the STP100D trigger input should be greater than 100 µsec and can be high going or low going. The MP system can be set up via Acq*Knowledge* to trigger on positive or negative edges.

Additionally, to use the STP100D external trigger in a manual mode, the input can be pulled low with an external switch connected between the trigger input and ground.

To externally trigger MP Unit acquisition, send a logic level signal to the External Trigger of the STP100D (TRIG). This line connects to the MP Unit External Trigger via optical isolation.

info@biopac.com
support@biopac.com
www.biopac.com

STP100D Instructions

1. Snap the STP100D module DSUB I/0 connectors on the left side of the AMI100D or HLT100C module.
2. Use the 3-meter ribbon cable to connect the STP100D module (computer I/O 37-pin connector or 25-pin parallel port) to the appropriate connector on the PC.

   For 37-pin connector:

   - Connects Port A (inputs; pins 37-30) on the digital I/O card to digital I/O lines 0-7 on the MP unit.
   - Connects Port B (outputs; pins 3-10) on the digital I/O card to digital I/O lines 8-15 on the MP unit.

   For 25-pin connector:

   - Connects status register (inputs; pins 10-13) on the parallel port to digital I/O lines 4, 5, 7, and 6 respectively in the MP unit.
   - Connects data register (outputs; pins 2-9) on the parallel port to digital I/O lines 8-15 on the MP unit.

3. Ground pins are:
   - 37-pin digital I/O cable (CBL110A): pins 19 and 21.
   - 25-pin parallel port cable (CBL110C): pins 18 and 25.

Application example — P300 visual evoked response test

To set up the STP100W with an MP System to perform a P300 visual evoked response test:

1. Connect two **SuperLab** outputs to the respective MP System digital inputs.
   - These **SuperLab** outputs are assigned to respective images that will be presented to the subject during the recording session. Typically, image presentation occurs within a statistical framework, i.e., *Image 1* is presented 20% of the time and *Image 2* is presented 80%. The **SuperLab** outputs will be tightly (1 ms) synchronized to the respective image presentation.
2. Set the MP System up to record EEG and the two **SuperLab** outputs, which should be directed to the MP System digital inputs.
3. After the recording session has been completed, use Acq*Knowledge* to perform specific averaging on the collected EEG data.
   a) Use the digital input corresponding to **SuperLab** output 1 as a “Control Channel” in the Find Peak Averaging Setup; all the responses resulting from *Image 1* presentation will be averaged together to create the composite response for *Image 1* presentation.
   b) Repeat the above procedure with the “Control Channel” assigned to **SuperLab** Output 2 to create the composite response for *Image 2* presentation.

For more information on setting up the **Find Cycle (Cycle Detector) Off-line Averaging** for this kind of measurement, see the Acq*Knowledge* Software Guide.pdf.